REMARKS

Claims 1-4 and 16-20 are all the claims presently being examined in the application. Claims 14 and 15 have been canceled above. Claims 1-4 and 16-20 stand rejected on prior art grounds.

Claim 18 stands rejected upon informalities under 35 U.S.C. § 112, first paragraph and second paragraph. Claims 1-3, 15, and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Enomoto, et al. Claim 14 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Enomoto, et al. as applied to claim 1 above, and further in view of Oura, et al. Claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Enomoto, et al. as applied to claim 1 above, and further in view of Kaskoun, et al. Claims 4, 18, and 19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kweon, et al. in view of Sakuma, et al. Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the acknowledged prior art of Fig. 1 in view of Kaskoun, et al.

These rejections are respectfully traversed in view of the following discussion.

Entry of this §1.116 Amendment is proper. Since the amendments above narrow the issues for appeal and since such features were in the claims earlier, such amendments do not raise a new issue requiring further searching and/or consideration by the Examiner. As such entry of this Amendment is believed to be proper and is earnestly solicited.

Attached hereto is a marked-up version of the changes made to the specification and/or claims by the current Amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE.**"

It is noted that the amendments are made only to more particularly define the

invention and not for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed, for example by independent claim 1, is directed to a semiconductor device.

The semiconductor device includes a semiconductor chip, a chip-mounting substrate which is provided with the semiconductor chip mounted on a top surface thereof and first conductive pads formed on a bottom surface thereof and connected with the semiconductor chip electrically, solder balls formed on the first conductive pads, a printed circuit board on which second conductive pads connected with the solder balls are formed, and material injected into a clearance formed between the chip-mounting substrate and the printed circuit board. An uneven roughness is formed on a surface which is brought into contact with the material of at least one of the chip-mounting substrate and the printed circuit board.

Specifically, the uneven roughness exists on a bottom surface of the chip-mounting substrate. The uneven roughness on the bottom surface increases an area of a contact surface between the chip-mounting substrate and an underfill material. (See Page 15, lines 1-4 and lines 23-28; Page 16, lines 13-19; Page 17, lines 3-9; and Figures 2-3).

A second embodiment, as disclosed and claimed, for example by independent claim 20, is also directed to a semiconductor device. The semiconductor device includes an uneven roughness formed on a contact surface of the Cu wiring between the Cu wirings of the

chip-mounting substrate and the solder balls. (See Page 17, lines 15-26; Page 20, lines 6-10; and Figures 5A-6B). Specifically, the uneven roughness exists on a bottom surface of the Cu wirings with the Cu wirings being connected to the solder balls to form a joined surface. (See Page 19, lines 1-4; and lines 15-24).

A third embodiment, as disclosed and claimed, for example by independent claim 4, is also directed to a semiconductor device. The semiconductor device includes an uneven roughness on a bottom surface of the lead frame. (See Page 20, lines 10-25; and Page 21, lines 18-Page 22, line 5; and Figures 9A and 9B).

Conventional semiconductor devices do not have an uneven roughness formed on a bottom surface of a chip-mounting substrate. However, this configuration tends to decrease in reliability because a reduction occurs in the adhesive strength of an underfill material due to contamination or external mechanical stresses thus causing the underfill material to exfoliate from the chip-mounting substrate or the printed circuit board. (See Page 1, line 22 - Page 2, line 24; and Figure 1).

An aspect of the present invention includes an uneven roughness on a bottom surface of the chip-mounting substrate. This configuration increases the contact area of the rough surface promoting greater adhesive strength between the chip-mounting substrate and the printed circuit board (according to claim 1). (See Page 4, line 17 through Page 5, line 4; and Page 15, line 23-28).

A very similar feature in a similar second embodiment of a semiconductor device, as disclosed and claimed, for example by independent claim 20, includes an uneven roughness exists on a bottom surface of the Cu wirings, which increases greater adhesive strength between the Cu wirings and the solder balls. (See Page 19, lines 1-4; and lines 15-24; Page 20, lines 10-25; and Page 21, lines 18-28).

A very similar feature in a similar third embodiment of a semiconductor device, as disclosed and claimed, for example by independent claim 4, includes an even roughness exists on a bottom surface of the lead frame, which increases greater adhesive strength between the lead frame and the printed circuit board. (See Page 20, lines 10-25; and Page 21, lines 18-28).

II. 35 USC § 112, First Paragraph and Second Paragraph, Rejections and Related Drawing Objection under 37 C.F.R. 1.83(a)

Applicant respectfully submits that the above amended claim 18 contains subject matter which was described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicant further respectfully submits that the above amended claim 18 particularly points and distinctly claims the subject matter of the invention, and thus fulfills the requirements of the 35 U.S.C. § 112, second paragraph.

Based on the above amended claim 18, Figures 9A and 9B show every feature of the invention as specified in amended claim 18 without entering new matter.

In view of the foregoing, the Examiner is respectfully requested to withdraw these rejections.

III. THE PRIOR ART REJECTION

A. The § 103(a) Rejection of Claims 1-3, 15 and 16.

First, the references, separately, or in combination, fail to teach, disclose or provide a motivation for being combined. In particular, the Prior Art pertains to semiconductor chips,

which are attached to printed circuit boards, not to producing printed circuit boards. The Prior Art also does not disclose, teach or suggest improving surface bonding. (See Column 2, lines 39-48; and Page 2, line 25 through Page 3, line 21).

The Prior Art discloses a semiconductor device, which includes a printed circuit board and a semiconductor chip mounting substrate with an underfill material but without an uneven roughness existing on a bottom surface of a chip-mounting substrate. The Prior Art is specifically directed to attempt solving the problem of the different thermal expansion coefficients between the printed circuit board and the chip mounting substrate by providing for an underfill material to absorb a stress caused by these expansions. (See Page 1, line 22-Page 2, line 25). However, the Prior Art devices have decreased reliability because a reduction occurs in the adhesive strength of an underfill material due to contamination or external mechanical stresses thus causing the underfill material to exfoliate from the chip-mounting substrate or the printed circuit board. (See Page 1, line 22 - Page 2, line 24; and Figure 1).

By contrast, Enomoto, et al. ("Enomoto') does not have the same aim as the Prior Art.

Enomoto's discloses an adhesive for electroless plating formed by dispersion of heat-resistant granules soluble in a heat resistant resin (See Enomoto at Abstract).

Enomoto is specifically directed to solving the drawbacks in the adhesive for electroless plating in producing the printed circuit boards (PCBs). Indeed, Enomot attempts to increase the adhesion property between a PCB and the patterns thereon. (See Column 1, lines 5-15; and Column 2, lines 38-48).

Nothing within Enomoto, which focuses on adhesives for electroless plating, has anything to do with underfill material for differences in thermal coefficients of expansion as disclosed in the Prior Art. Thus, the Prior Art teaches away from being combined with

another invention, such as, Enomoto.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight. It is clear that the Examiner has simply read Applicant's specification and conducted a keyword search to yield the Prior Art and Enomoto. Further, the Examiner provides no motivation or reason to combine other than to assert that it would have been obvious to one having ordinary skill in the art at the time to modify the Prior Art with Enomoto. Such an assertion does not take into account the distinct structural differences of the Prior Art as indicated above, and further discussed below. Thus, the Examiner's assertion attempts to solve a potential problem which does not ever exist with the Prior Art, and this assertion is further proof of the Examiner's use of impermissible hindsight.

Second, even if combined, the references do not teach or suggest the features of independent claim 1. Specifically, there is no teaching or suggestion of at least that the uneven roughness exists on a bottom surface of the chip-mounting substrate, let alone, the uneven roughness on the bottom surface increases an area of a contact surface between the chip-mounting substrate and an underfill material .

Examiner admits that the Prior Art and Enomoto do not disclose, teach or suggest at least one element of the claimed invention, including "the uneven roughness existing on a bottom surface of the chip-mounting substrate." (See Office Action, Page 5, Section 10).

To make up for the deficiencies of the Prior Art and Enomoto, the Examiner relies on Oura, et al. ("Oura"). Oura fails to do so.

First, Oura does not have the same aim as either the Prior Art or Enomoto as discussed above, and the combination would not have been made absent hindsight.

Oura is specifically directed to solve the problem of bonding an electroless plating on a resin material by providing for "a resin structure to manufacture an electric circuit device in

which it can be bonded onto a resin layer by directly electroless plating and the mechanical strength is sufficiently high" at low cost. (See Column 4, lines 8-26). Oura further relates to the resin substrate serving as an interposer where the surface of the interposer, which has a roughness, is bonded to an IC chip situated on top of the interposer. (See Column 31, lines 5-19).

Nothing within Oura has anything to do with a semiconductor device, which includes a printed circuit board and a semiconductor chip mounting substrate with an underfill material, to attempt solving the problem of the different thermal expansion coefficients between the printed circuit board and the chip mounting substrate and absorb a stress caused by these expansions as disclosed in the Prior Art. (See Page 1, line 22- Page 2, line 25).

Similarly, nothing within Oura has anything to do with solving the drawbacks in the adhesive for electroless plating in producing printed circuit boards (PCBs) and improving the adhesion property between a PCB and the patterns thereon through an adhesive for electroless plating formed by dispersion of heat-resistant granules soluble in a heat resistant resin as disclosed in Enomoto. Thus, the Prior Art and Enomoto teach away from being combined with each other as well another invention, such as, Oura.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight.

Second, even if combined, the references do not teach or suggest the features of independent claim 1, and incorporated previous claim 14, including an uneven roughness exists on a bottom surface of the chip-mounting substrate.

Oura does not make up for the deficiencies of either the Prior Art or Enomoto as discussed above. Instead, Oura discloses a a resin structure, which includes a resin layer and a metal layer. The resin layer, which has a roughness, is formed of a single material and the

metal layer is laminated directly on the resin layer without the intervention of an adhesive layer (See Oura at Abstract; Column 1, lines 5-13; and Column 4, lines 27-35). The resin substrate serves as an interposer where the surface of the interposer is bonded to an IC chip situated on top of the interposer without an uneven roughness formed on a surface which is brought into contact with the material of at least one of the chip-mounting substrate and the printed circuit board, let alone, the uneven roughness existing on a bottom surface of a chip-mounting substrate as disclosed in Applicant's invention (See Column 31, lines 5-19).

Oura also does not disclose or suggest the uneven roughness on the bottom surface increases an area of a contact surface between the chip-mounting substrate and the underfill material also as taught by Applicant's invention.

The Applicant traverses the assertion in the Office Action that Oura in Figure 34 discloses "an uneven roughness existing on a bottom surface of a chip-mounting substrate (191)." (See Office Action at Page 5). Although Oura discloses a roughness on an upper surface of a resin substrate, i.e., the interposer, for bonding with an IC chip, this configuration is supposedly designed to "minimize the trouble that the IC chip is stripped from the boundary between the adhesive and the interposer" (See Column 31, lines 5-20). In contrast, Applicant teaches that the uneven roughness is on a bottom surface of a chip-mounting substrate. Since the uneven roughness is formed on the bottom surface of the chip-mounting substrate, the rough surface promotes greater adhesive strength between the chip-mounting substrate and the printed circuit board reducing exfoliation with the underfill material (See Page 4, line 17 through Page 5, line 4; and Page 15, line 23-28). Oura, however, does not disclose a semiconductor device, including the uneven roughness exists on a bottom surface of said chip-mounting substrate (See Page 15, lines 1-4 and lines 23-28; Page 16, lines 13-19; Page 17, lines 3-9; and Figures 2-3). Consequently, Oura does not teach, suggest or

disclose Applicant's invention.

Therefore, none of the Prior Art, Enomoto and Oura teaches or suggests a semiconductor device which includes the uneven roughness exists on a bottom surface of the chip-mounting substrate as recited in claim 1, i.e., Applicant's invention. The invention provides a semiconductor device, which provides an uneven roughness on a bottom surface of the chip-mounting substrate, effectively increases the contact area of the rough surface promoting greater adhesive strength between the printed circuit board and the chip mounting substrate, which reduces exfoliation of the underfill material from the chip-mounting substrate and the printed circuit board, thereby increasing the reliability of the semiconductor device operating in the electronic circuit. (See Page 4, line 17 through Page 5, line 4; and Page 15, line 23-28; Page 15, line 28-Page 16, line 4; Page 19, lines 15-24; and Page 22, lines 4-5).

For at least the reasons outlined above, Applicant respectfully submits that none of the Prior Art, Enomoto, and Oura teach or suggest all of the features of the independent claim 1 and incorporated dependent claim 14.

For the reasons stated above, the claimed invention, and the invention as cited in independent claim 1, should be fully patentable over the cited references.

C. The Kaskoun Reference

Regarding claim 17, Kaskoun, et al. ("Kaskoun") fails to make up for the deficiencies of the Prior Art and Enomoto.

Further, Kaskoun does not teach or suggest a semiconductor device, where a surface of the chip-mounting substrate has a slit-like shaped configuration as recited in claim 17 of the invention.

For the reasons stated above, the claimed invention, and the invention as cited in

independent claim 1, and related claim 17, should be fully patentable over the cited references.

D. The § 103(a) Rejection Based on Kweon et al. in View of Sakuma et al.

First, the references separately, or in combination, fail to teach, disclose or provide a motivation for being combined. In particular, Kweon, et al. ("Kweon") pertains to a packaging structure for a surface mounting type semiconductor package with at least one semiconductor chip mounted on a die pad where a conductive pattern is formed on a printed circuit board located beneath an exposed side of a die pad of the package (See Kweon at Abstract; and Column 1, lines 10-23).

Kweon is specifically directed to, "improve the grounding property by the particular packaging structure, which allows a reduction of the noise, without deteriorating the operation speed or mounting density of the package" by providing "a nonconductive thin film as a capacitor formed in a space between the die pad and the conductive pattern where the space has a voltage difference." (See Column 3, lines 8-33).

By contrast, Sakuma, et al. ("Sakuma") does not have the same aim as Kweon.

Sakuma discloses a circuit substrate for use in manufacturing integrated circuit devices by the strip-support method in connection with a semiconductor element having conductive pads. The circuit substrate includes bumps on the finger leads with a specified surface roughness for connection with the conducting leads of a semiconductor element to be mounted on the circuit substrate (See Sakuma at Abstract; and Column 1, lines 5-24).

Sakumo is specifically directed to the mounting of a semiconductor silicon chip and to "provide an improved method for forming the bumps on the conductive layers of the circuit substrates where the positioning error of the bumps on the finger leads are prevented" and "provide a circuit substrate with bumps having a roughness of between 5 and 15 microns to

improve connection of the circuit substrate structure to the conductive pad of the IC chip" (See Column 2, lines 60-66; Column 3, lines 41-46).

Nothing within Sakuma, which relates to reliable formation of a desirable pattern, has anything to do with a low noise packaging structure for a surface-mounting type semiconductor package, including a nonconductive thin film as a capacitor formed in a space between the die pad and the conductive pattern where the space has a voltage difference as disclosed in Kweon. Kweon also does not appear to disclose or teach an improved method for forming the bumps on the conductive layers of the circuit substrates. Thus, Kweon teaches away from being combined with another invention, such as Sakuma.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight. It is clear that the Examiner has simply read Applicant's specification and conducted a keyword search to yield Kweon and Sakuma. Further, the Examiner provides no motivation or reason to combine other than to assert that it would have been obvious to one having ordinary skill in the art at the time to modify Kweon with the uneven rough contact surfaces in direct contact between the lead frame and the printed circuit board of Sakuma to improve the connection between the lead frame and the printed circuit board. Such an assertion does not take into account the distinct structural differences of Kweon as indicated above, and further discussed below. Thus, the Examiner's assertion attempts to solve a potential problem which does not ever exist with Kweon, and this assertion is further proof of the Examiner's use of impermissible hindsight.

Second, even if combined, the references do not teach or suggest the features of independent claim 4. Specifically, there is no teaching or suggestion of at least that the uneven roughness exists on a bottom surface of the lead frame.

Examiner indicates that Kweon does not disclose, teach or suggest at least two

elements of the claimed invention, including, "at least one of the lead frame and the printed circuit board is provided with uneven rough contact surfaces in direct contact therebetween." (See Office Action at Page 7). Kweon also does not disclose that "the uneven roughness exists on a bottom surface of the lead frame."

Separately, Sakuma discloses a circuit substrate for use in manufacturing integrated circuit devices by the strip-support method in connection with a semiconductor element having conductive pads. The circuit substrate includes a bump on a back surface of a conducting pattern indirectly connected to a circuit substrate base film with an adhesive layer situated between the bump and a circuit base film without at least one of the lead frame and the printed circuit board provided with uneven rough contact surfaces in direct contact therebetween, let alone, the uneven roughness exists on a bottom surface of the lead frame. (See Sakuma at Abstract; Column 4, lines 50-60; Column 7, lines 20-31; and Figure 7). Accordingly, Applicant traverses the assertion in the Office Action that Figure 7 of Sakuma discloses "at least one of a lead frame (3) and a printed circuit board being provided with uneven rough contact surfaces in direct contact therebetween." (See Office Action at Page 7, lines 6-8).

Instead Sakuma discloses an indirect connection through the use of an adhesive layer situated between the bump and the circuit base film to increase bonding not a direct connection where outer leads of a lead frame with an uneven roughness are connected to the conductive pads of the printed circuit board by thermal compression welding as indicated in Applicant's invention (See Column lines 50-60; and Sakuma, Page 21, lines 18-23). Since Sakuma uses an adhesive layer, cracking may likely occur between the bump and the circuit base film. Consequently, Sakuma's conventional structure is unsuitable for achieving at least two objects of the invention, which provides a lead frame and the printed circuit board

provided with uneven rough contact surfaces in direct contact therebetween, to increase the contact area of the rough surface promoting high adhesive strength between the printed circuit board and the outer leads of the lead frame. This configuration prevents cracking of the joined surface between the lead frame and the printed circuit board caused by mechanical or thermal impacts, thereby increasing the reliability of the semiconductor device operating in the electronic circuit. (See Page 21, lines 18-Page 22, line 5 and lines 12-13). Sakuma does not teach, suggest or disclose a semiconductor device, including at least one of the lead frame and the printed circuit board provided with uneven rough contact surfaces in direct contact therebetween, and, the uneven roughness exists on a bottom surface of the lead frame.

Therefore, Kweon and/or Sakuma fail to teach or suggest Applicant's invention, as defined by independent claim 4.

Regarding dependent claims 18 and 19, which depend from independent claim 4, these claims are patentable not only by virtue of their dependency from the respective independent claim, but also by the additional limitations they recite.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

E. The § 103(a) Rejection of Claim 20

Kaskoun, et al. ("Kaskoun") does not have the same aim as the Prior Art as discussed above.

Kaskoun discloses a fluxless flip-chip bond and a related method for flip-chip bonding of two electronic components without the use of a flux material. The method includes a substrate of one electronic component is roughened to provide an improved adhesive surface for a solder ball. (See Kaskoun at Abstract; and Column 1, lines 5-8).

Kaskoun is specifically directed to solve the problems of assemblying electronic components, which involve residual flux material, heat dissipation in the packaging and tacking pressure, by providing for "an improved method for bonding electronic components that does not require the use of a flux material, that eliminates the risks of deforming the solder balls and does not add appreciable complexity or cost to the manufacturing process (See Column 1, lines 25-63). Nothing within Kaskoun has anything to do with a semiconductor device, which includes a printed circuit board and a semiconductor chip mounting substrate with an underfill material, to attempt solving the problem of the different thermal expansion coefficients between the printed circuit board and the chip mounting substrate and absorb a stress caused by these expansions as disclosed in the Prior Art. (See Page 1, line 22- Page 2, line 25). Thus, the Prior Art teaches away from being combined with another invention, such as, Kaskoun.

Therefore, one of ordinary skill in the art would not have combined these references, absent hindsight. It is clear that the Examiner has simply read Applicant's specification and conducted a keyword search to yield the Prior Art and Kaskoun. Further, the Examiner provides no motivation or reason to combine other than to assert that it would have been obvious to one having ordinary skill in the art at the time to modify the Prior Art with Kaskoun "to use the uneven rough contact surface of Kaskoun et al. in the device of the acknowledged prior art of Fig. 1 in order to provide a reliable contact" (See Office Action at Page 8). Such an assertion does not take into account the distinct structural differences of the Prior Art as indicated above, and further discussed below. Thus, the Examiner's assertion attempts to solve a potential problem which does not ever exist with the Prior Art, and this assertion is further proof of the Examiner's use of impermissible hindsight.

Second, even if combined, the references do not teach or suggest the features of

independent claim 20. Specifically, there is no teaching or suggestion of at least that an uneven roughness is formed on a contact surface between the Cu wirings of the chip-mounting substrate and the solder balls, let alone, where the uneven roughness exists on a bottom surface of the Cu wirings, and the Cu wirings are connected to the solder balls to form a joined surface.

Kaskoun does not make up for the deficiencies of the Prior Art as discussed above. Instead, Kaskoun, as indicated above, discloses a fluxless flip-chip bond and a related method for flip-chip bonding of two electronic components without the use of a flux material. The method includes a substrate of one electronic component is roughened to provide an improved adhesive surface for a solder ball. The roughened pattern is replicated by additional conductive layers formed over the substrate or formed on one of the intermediary or top conductive layers. (See Kaskoun at Abstract; and Column 1, lines 5-8; and Column 2, lines 29-57).

Applicant traverses the assertion in the Office Action that Kaskoun in Figure 1 discloses "uneven roughness being formed on a contact surface between said Cu wirings (17) of said chip-mounting substrate and said solder balls (12)" (See Office Action at Page 8). Kaskoun discloses a copper layer with a nickel layer on top of the copper layer with a gold layer on top of the nickel layer. The gold layer with an upper roughened pattern is brought in contact with the solder ball oriented on top of the gold layer not copper wiring in direct contact with the solder ball where the uneven roughness exists on a bottom surface of the Cu wirings, and the Cu wirings are connected to the solder balls to form a joined surface as disclosed in Applicant's invention (See Kaskoun, Column 3, lines 31-48; Column 4, lines 40-52; and Figure 1). Kaskoun also discloses a substrate over a bonding pad where a solder ball is formed on the bonding pad. The "bonding pad is an interfacial layer between substrate

26 of the first electronic component 27 and solder ball 12." "The function of bonding pad 11 is to provide adhesion for a solder ball 12 which is formed on bonding pad 11." (See Column 2, lines 33-52). Accordingly, Kaskoun does not disclose, teach or suggest that an uneven roughness exists on a bottom surface of the Cu wirings, and the Cu wirings are connected to the solder balls to form a joined surface.

In contrast, Applicant teaches that the uneven roughness exists on a bottom surface of the Cu wirings, and the Cu wirings are connected to the solder balls to form a joined surface. Since the uneven roughness is formed on the bottom surface of the chip-mounting substrate, the rough surface promotes greater adhesive strength between the chip-mounting substrate and the printed circuit board reducing exfoliation with the underfill material (See Page 4, line 17 through Page 5, line 4; and Page 15, line 23-28). Kaskoun, however, does not disclose a semiconductor device, including the uneven roughness exists on a bottom surface of the chip-mounting substrate (See Page 15, lines 1-4 and lines 23-28; Page 16, lines 13-19; Page 17, lines 3-9; and Figures 2-3). Consequently, Kaskoun does not teach, suggest or disclose Applicant's invention.

Therefore, neither the Prior Art nor Kaskoun teaches or suggests a semiconductor device which includes the uneven roughness exists on a bottom surface of the chip-mounting substrate as recited in claim 20, i.e., Applicant's invention.

For at least the reasons outlined above, the claimed invention cited in independent claim 20, should be fully patentable over the cited references.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1- 4 and 16-20, all the claims

presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 14 and 15 were canceled without prejudice or disclaimer.

The claims were amended as follows:

1. (Amended) A semiconductor device, comprising:

a semiconductor chip;

a chip-mounting substrate which is provided with said semiconductor chip mounted on a top surface thereof and first conductive pads formed on a bottom surface thereof and connected with said semiconductor chip electrically;

solder balls formed on said first conductive pads;

a printed circuit board on which second conductive pads connected with said solder balls are formed; and

underfill material injected into a clearance formed between said chip-mounting substrate and said printed circuit board,

wherein uneven roughness is formed on a surface which is brought into contact with said material of at least one of said chip-mounting substrate and said printed circuit board,

wherein said uneven roughness exists on a bottom surface of said chip-mounting substrate, and

wherein said uneven roughness on said bottom surface increases an area of a contact surface between said chip-mounting substrate and the underfill material.

2.(Amended) A semiconductor device according to claim 1, wherein[;] said uneven roughness is formed on at least one of said first conductive pads [or] and said second

conductive pads selectively.

3. (Amended) A semiconductor device according to claim 1, wherein[;] said uneven roughness is shaped into at least one of a slit-like configuration [or into] and a dimple-like configuration.

4. (Amended) A semiconductor device, comprising:

a semiconductor chip;

a lead frame which is provided with said semiconductor chip mounted thereon and electrically connected with said semiconductor chip; and

a printed circuit board including third conductive pads which are formed thereon and brought into direct contact with said lead frame,

wherein at least one of said lead frame and said printed circuit board is provided with uneven rough contact surfaces in direct contact therebetween, and

wherein said uneven roughness exists on a bottom surface of said lead frame.

18. (Amended) The semiconductor device according to claim 4, wherein said [semiconductor chip is provided with a chip-mounting substrate] lead frame comprises a lead, said lead comprises an inner lead portion connected to an outer lead portion, said outer lead portion comprises said uneven roughness.

20. (Amended) A semiconductor device, comprising:

a semiconductor chip;

a chip-mounting substrate which is provided with said semiconductor chip mounted

on a top surface thereof and first conductive pads formed on a bottom surface thereof and connected with said semiconductor chip electrically, said chip-mounting substrate including Cu wirings;

solder balls formed on said first conductive pads;

a printed circuit board on which second conductive pads connected with said solder balls are formed; and

material injected into a clearance formed between said chip-mounting substrate and said printed circuit board,

wherein uneven roughness is formed on a contact surface between said Cu wirings of said chip-mounting substrate and said solder balls, and

wherein said uneven roughness exists on a bottom surface of said Cu wirings, and said Cu wirings are connected to said solder balls to form a joined surface.